

FIG. 2

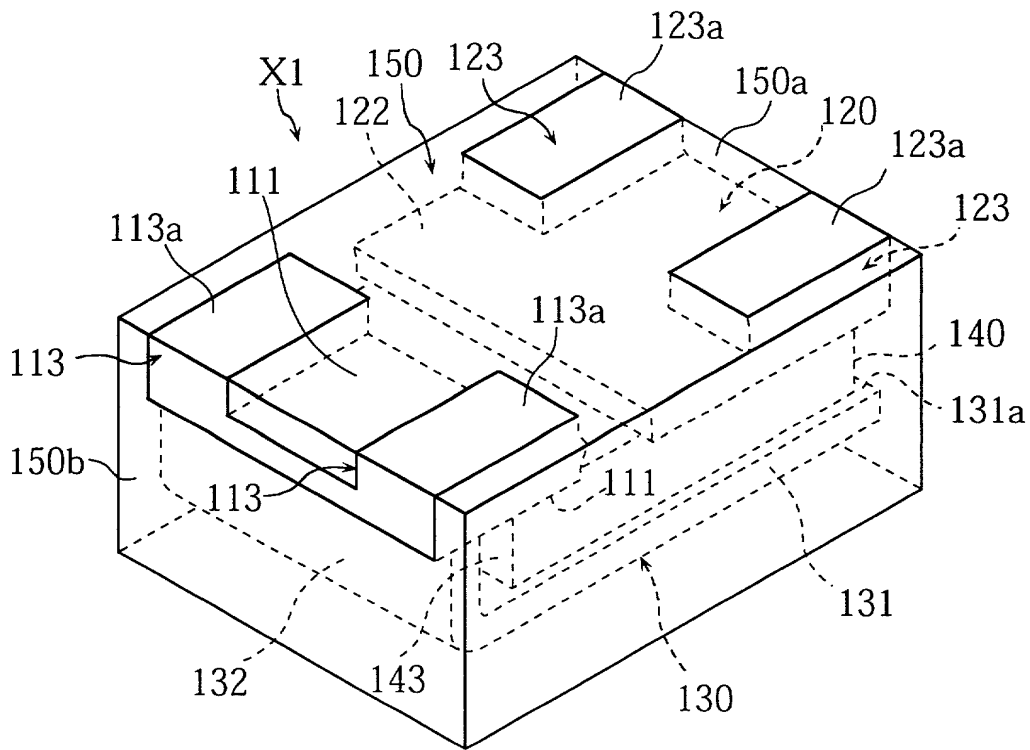


FIG. 3

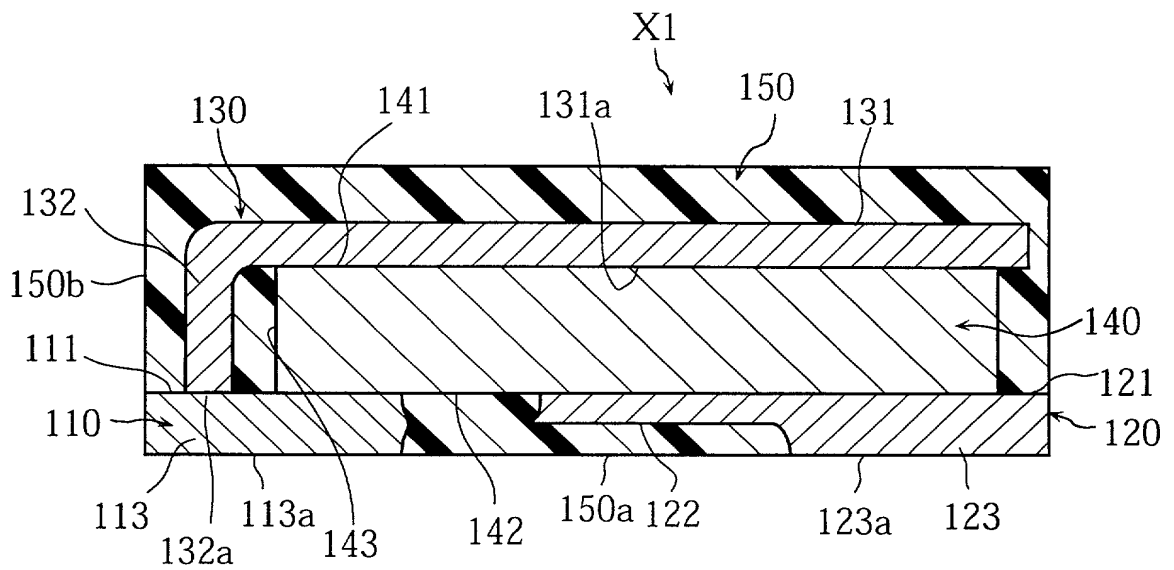
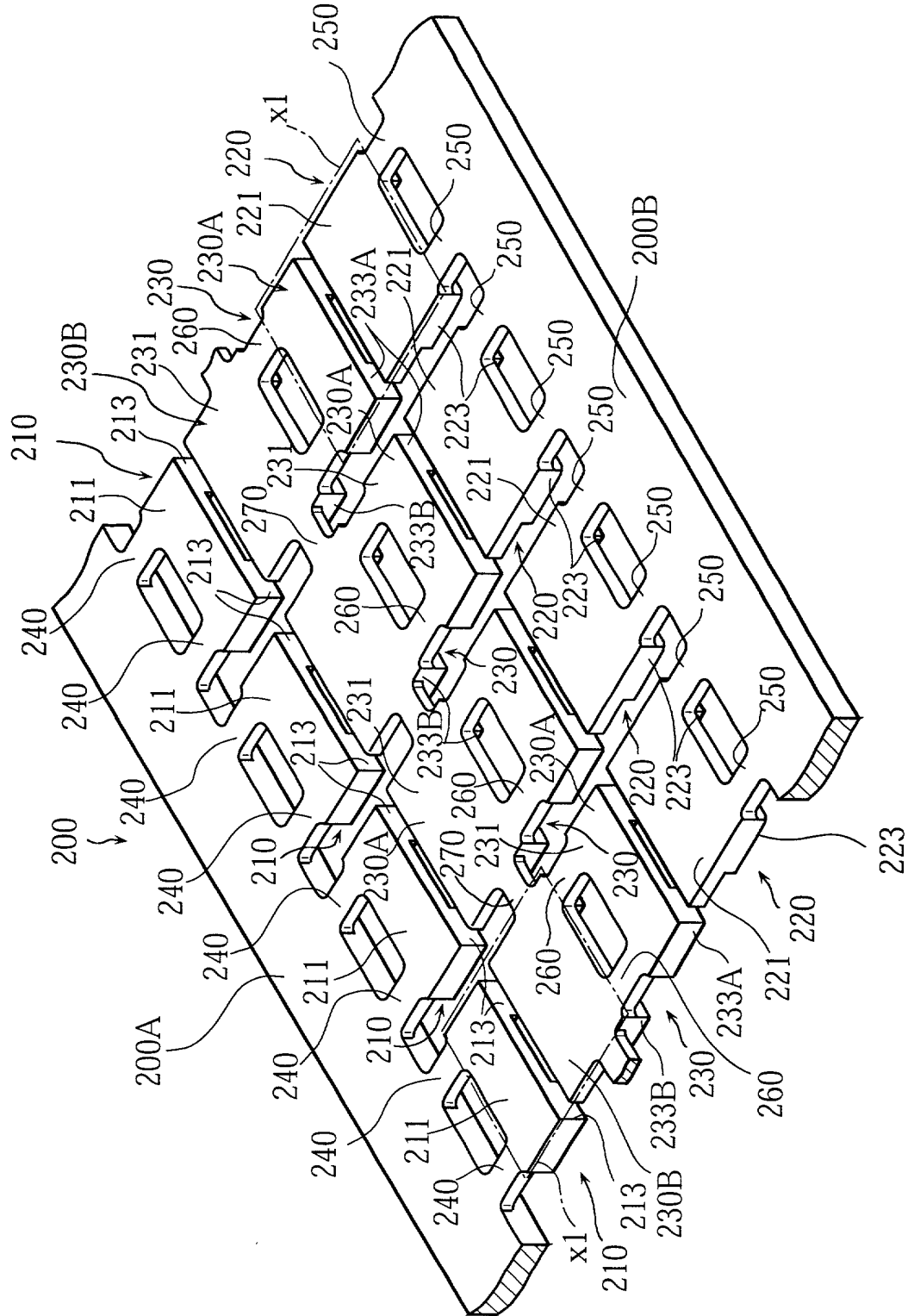


FIG. 4



[illegible]

FIG. 6

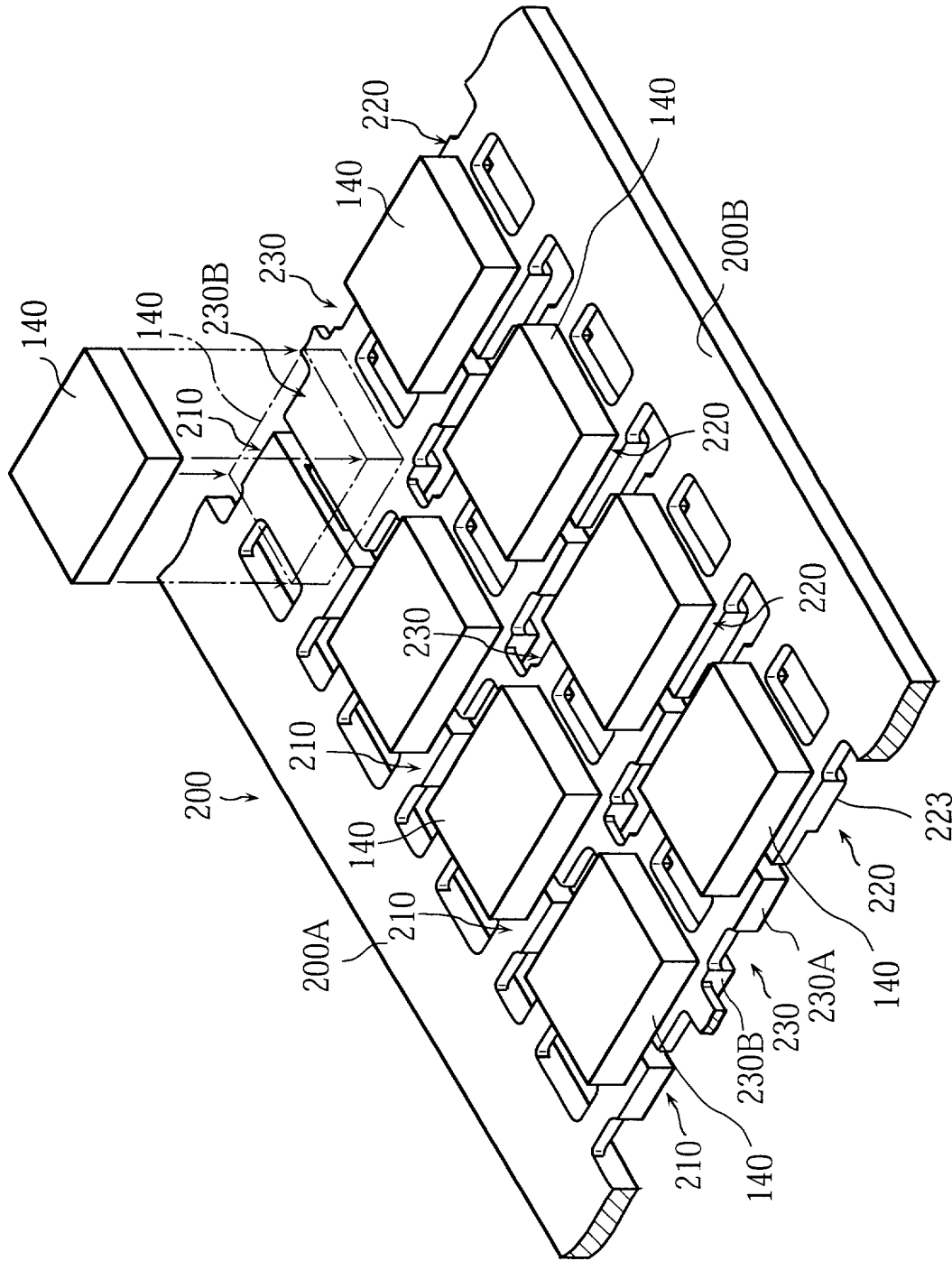


FIG. 7

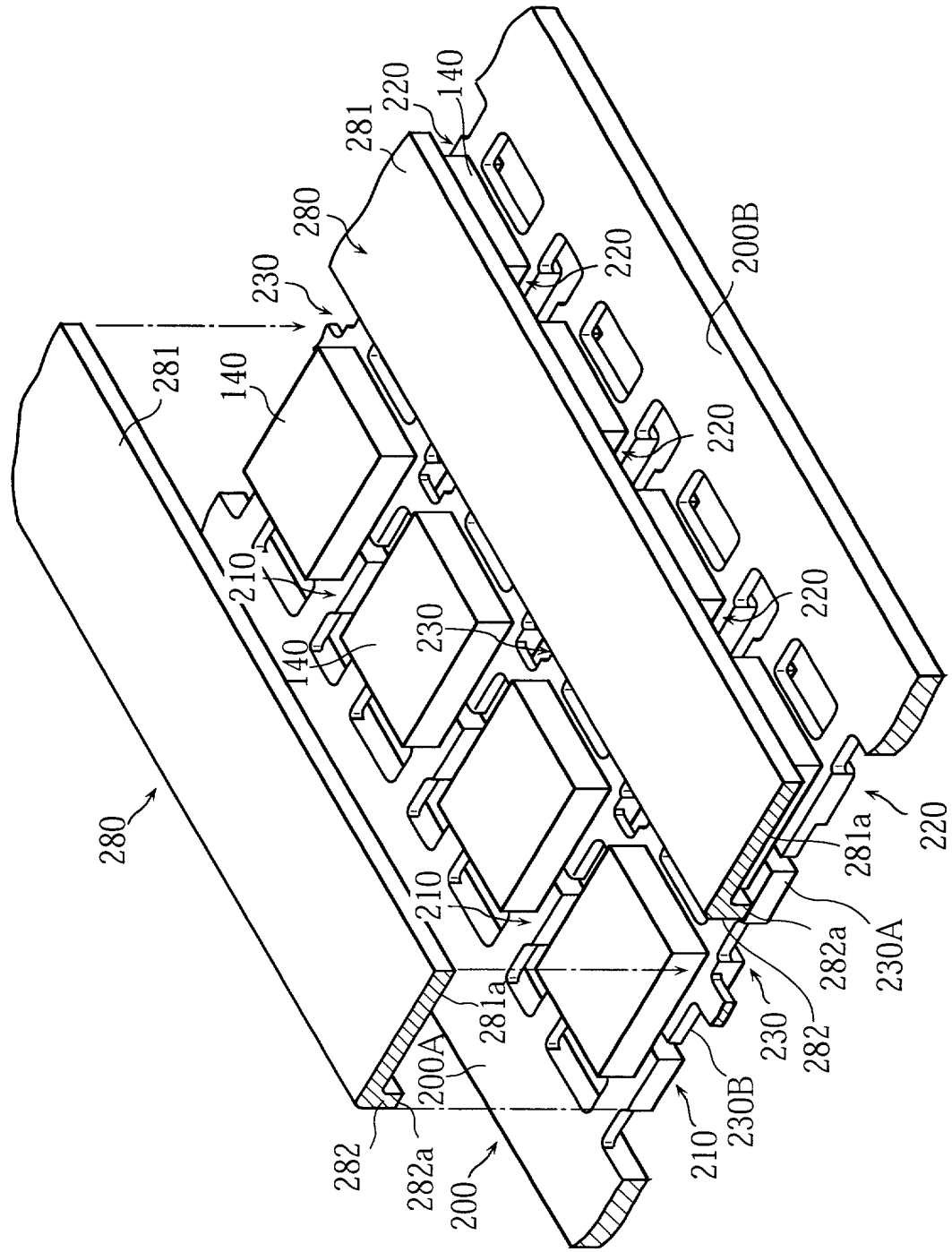


FIG. 8

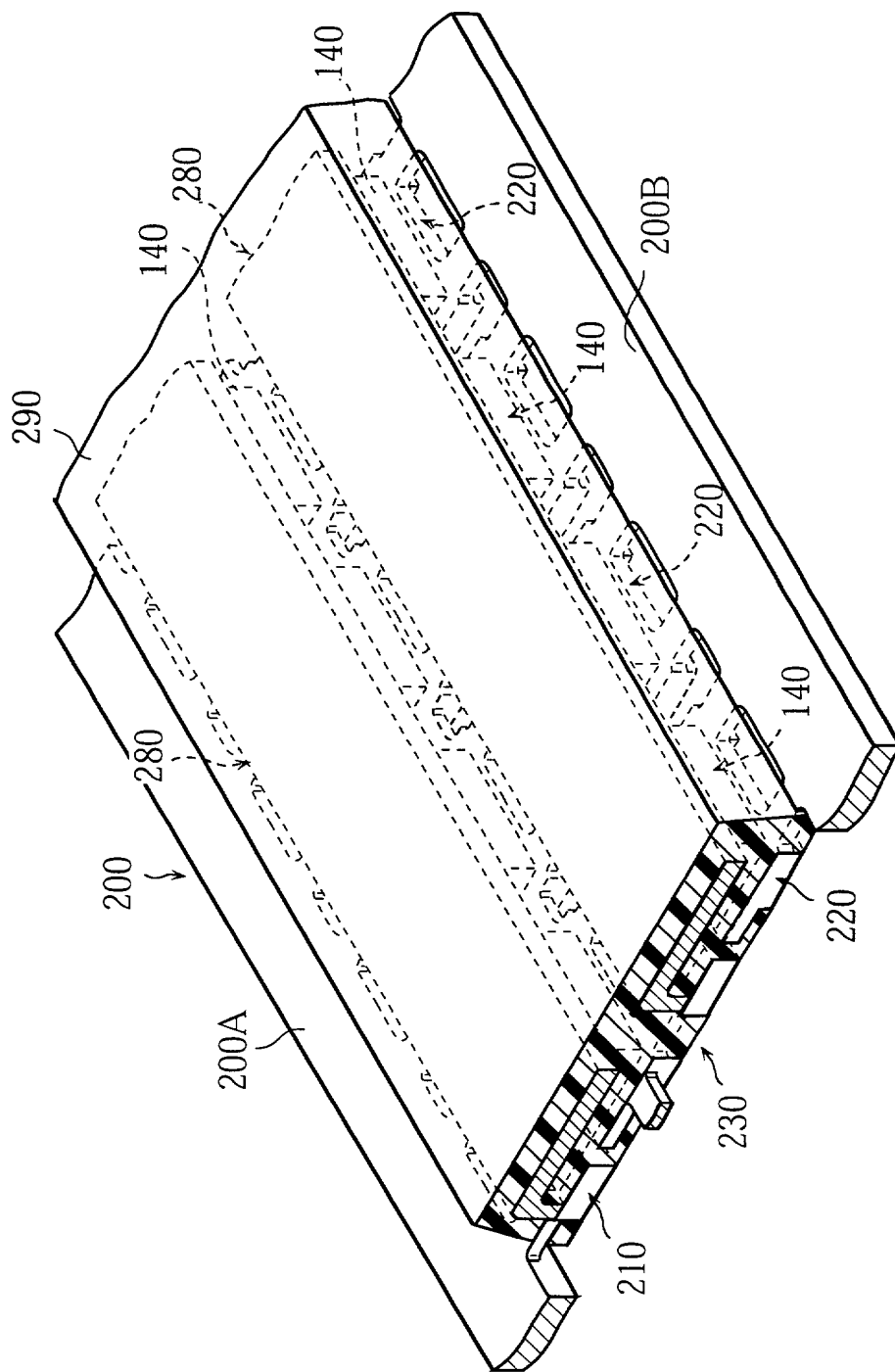


FIG. 9

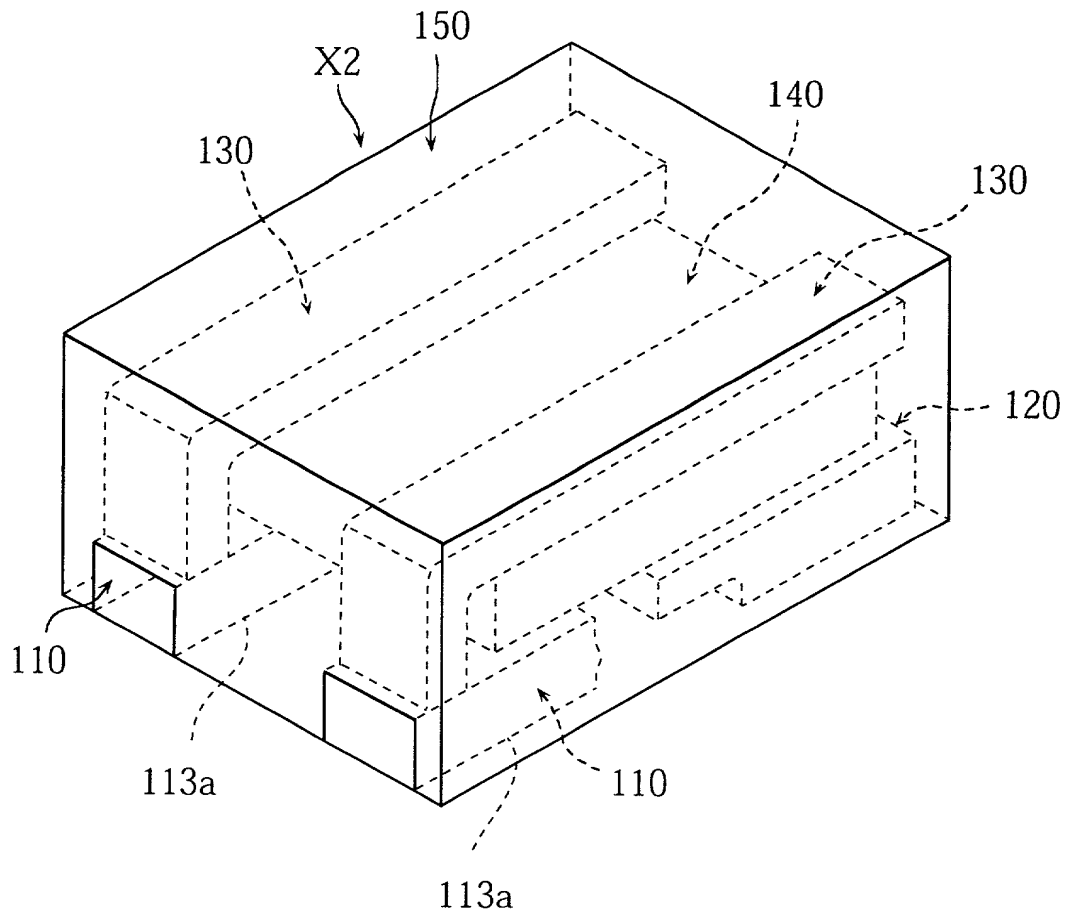


FIG. 10

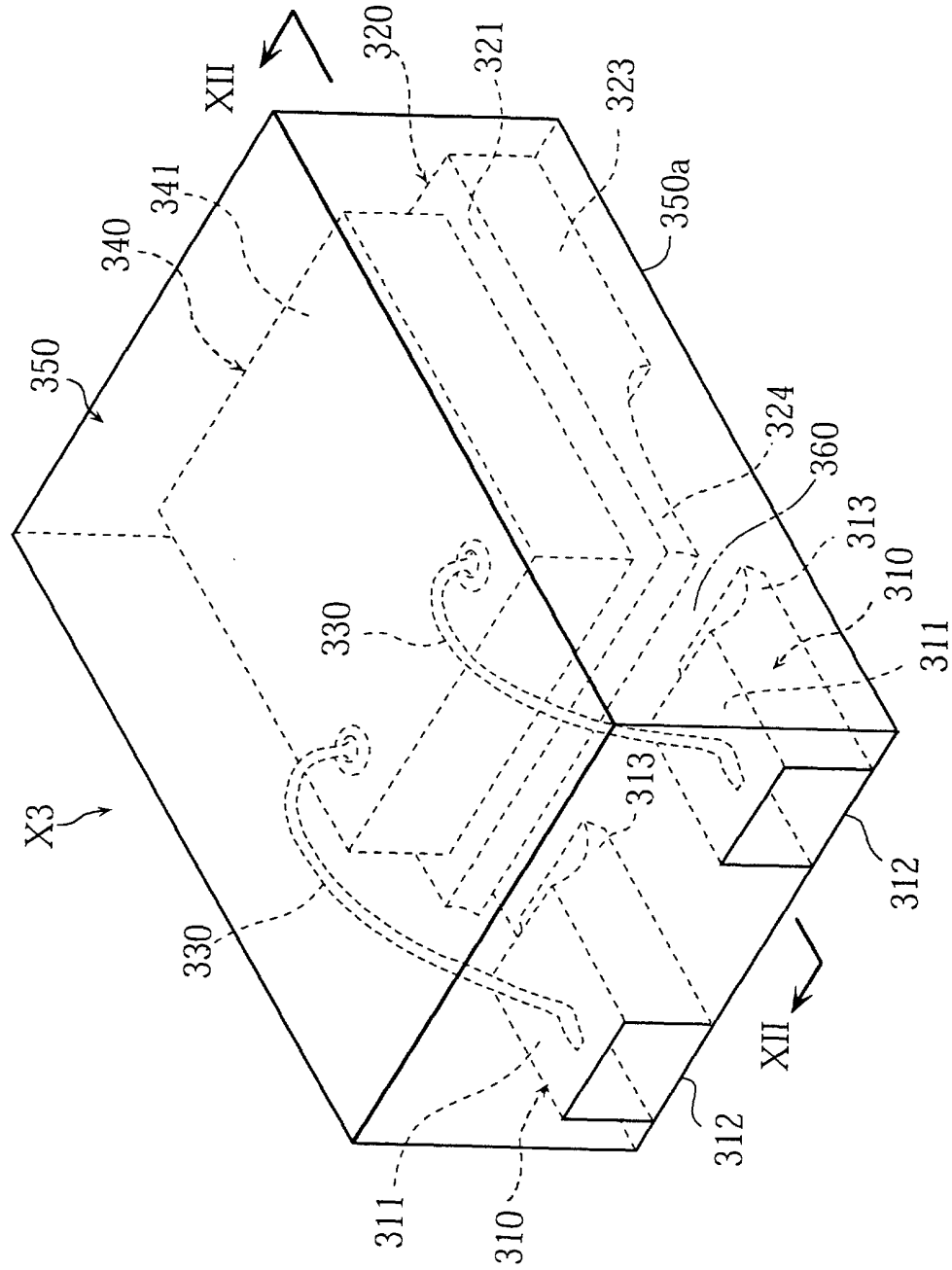


FIG. 11

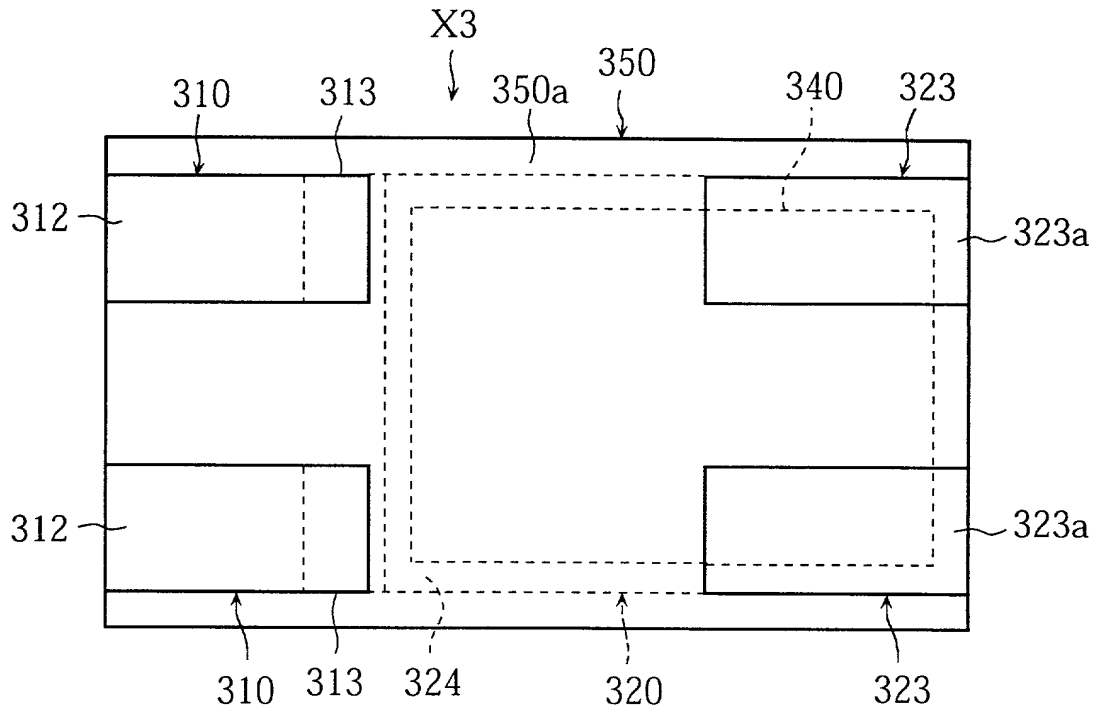


FIG. 12

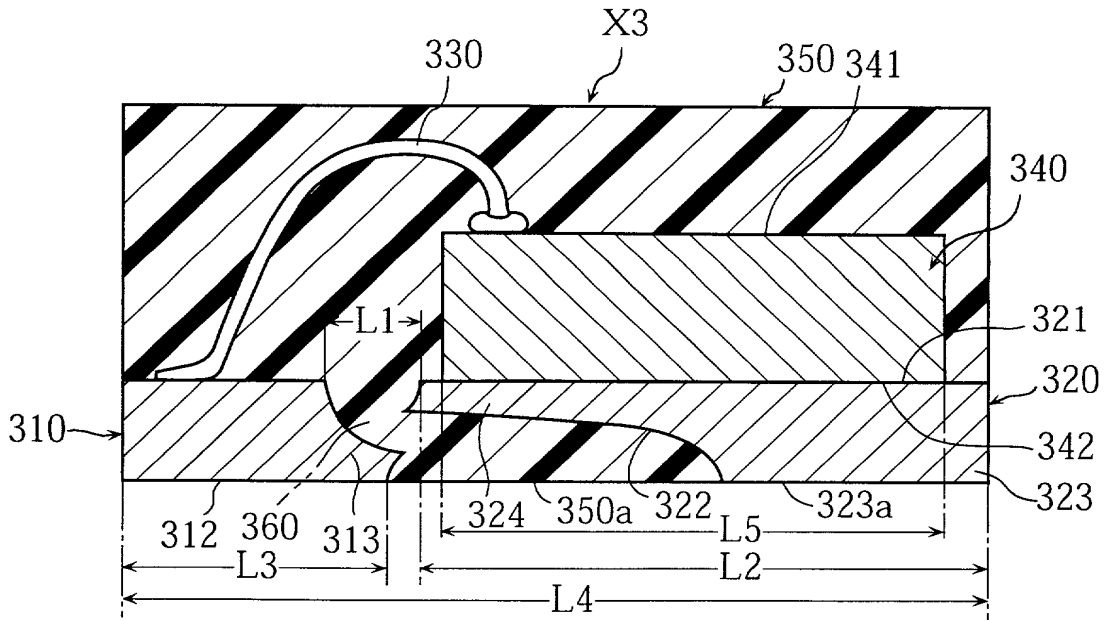


FIG. 13

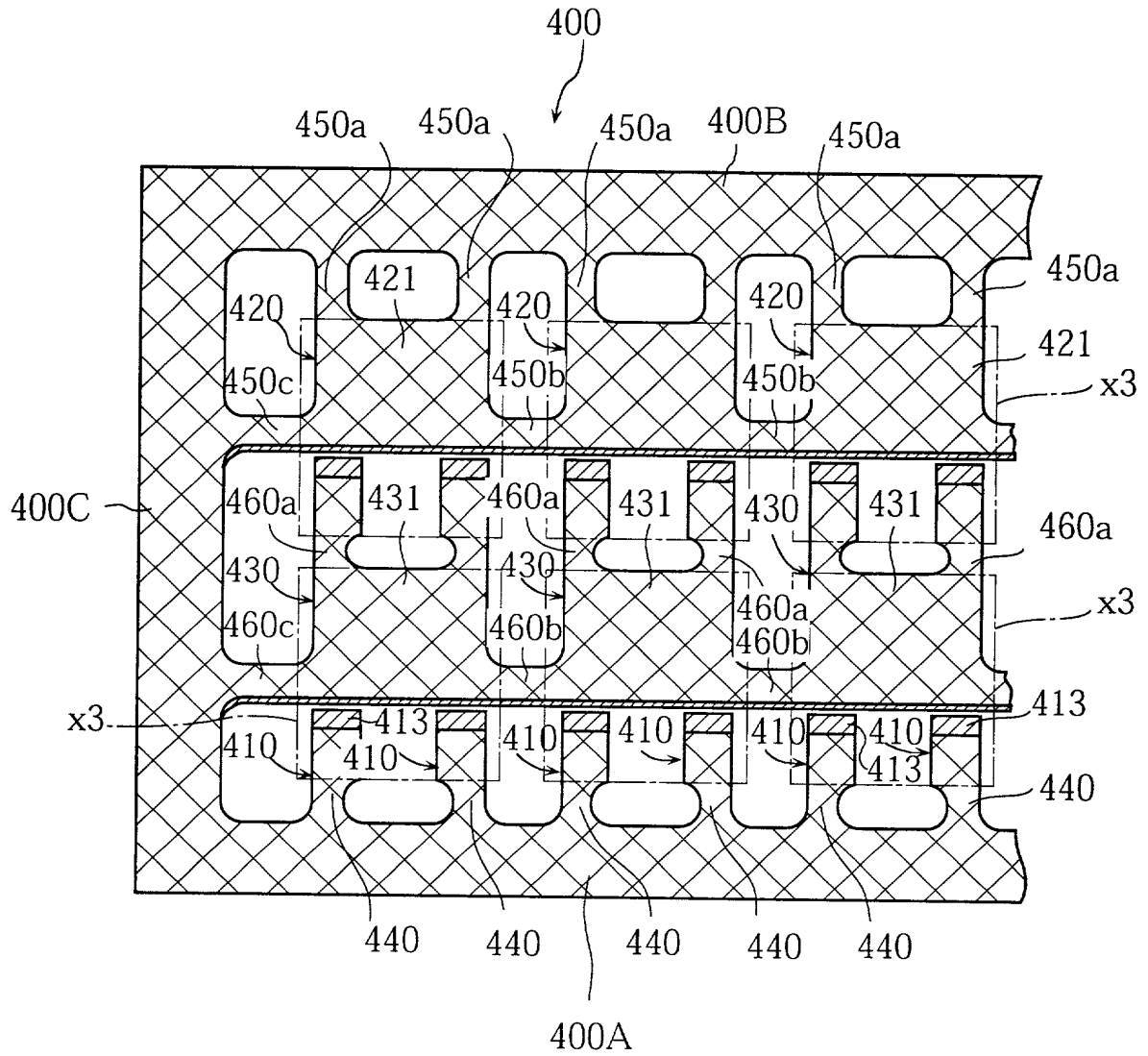


FIG. 14

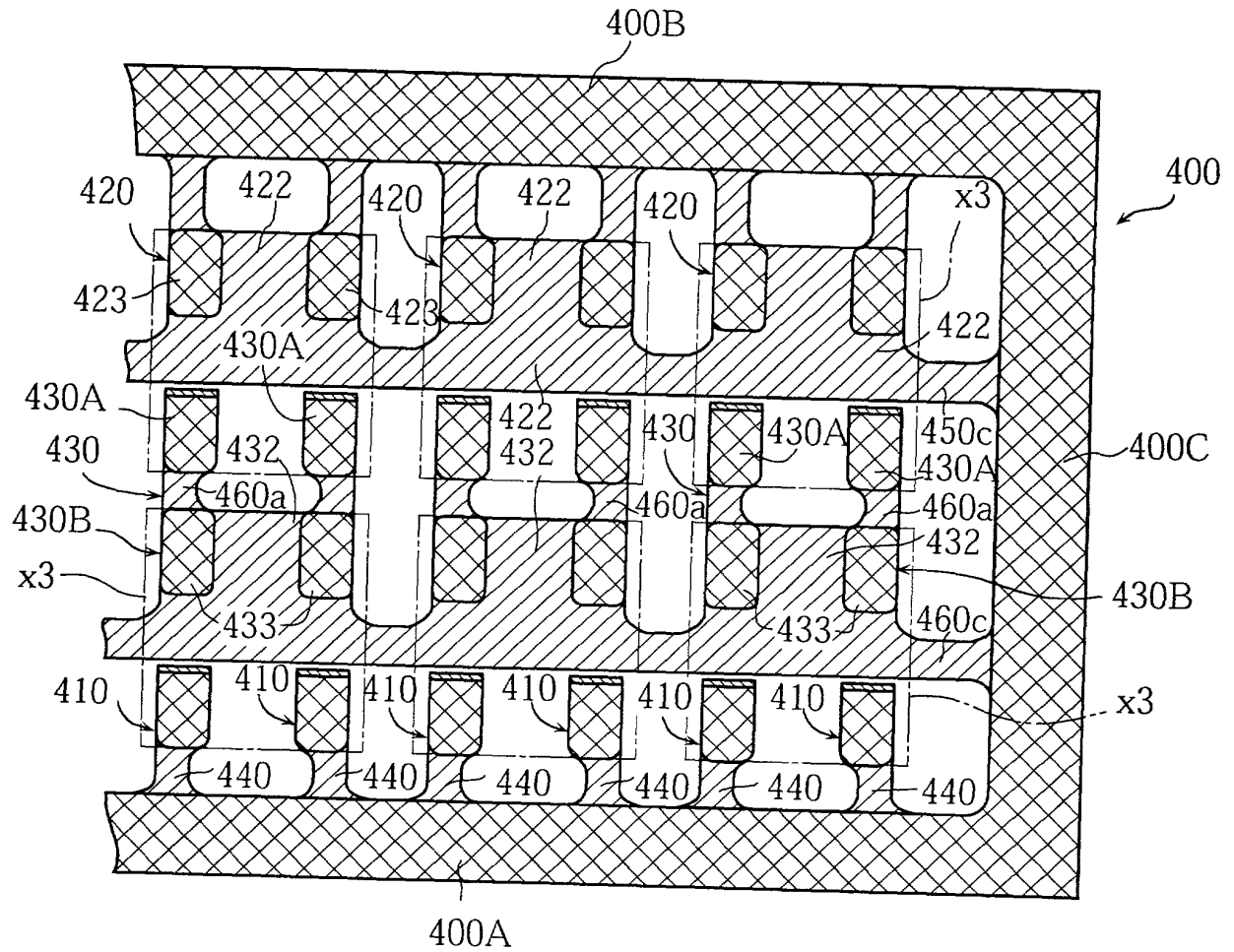


FIG. 15A

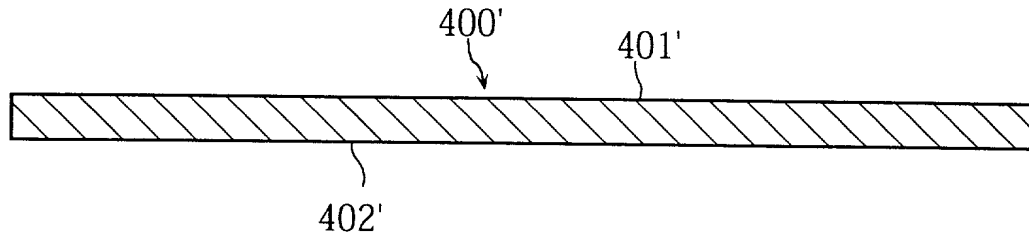


FIG. 15B

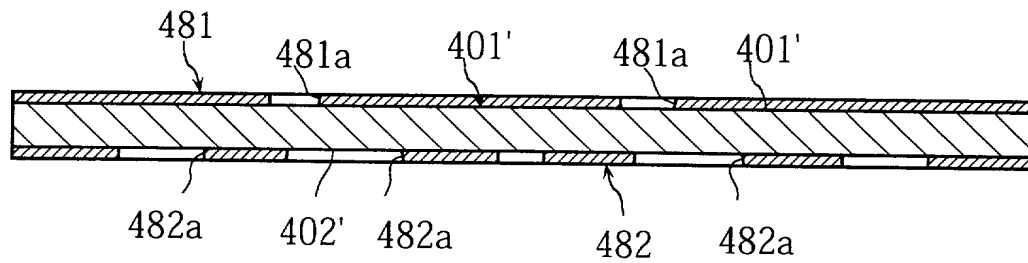


FIG. 15C

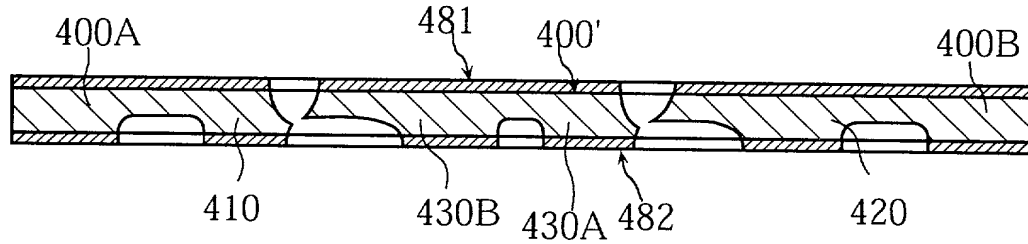


FIG. 15D

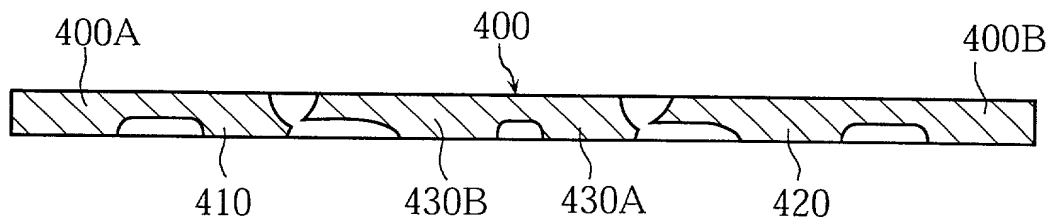


FIG. 16

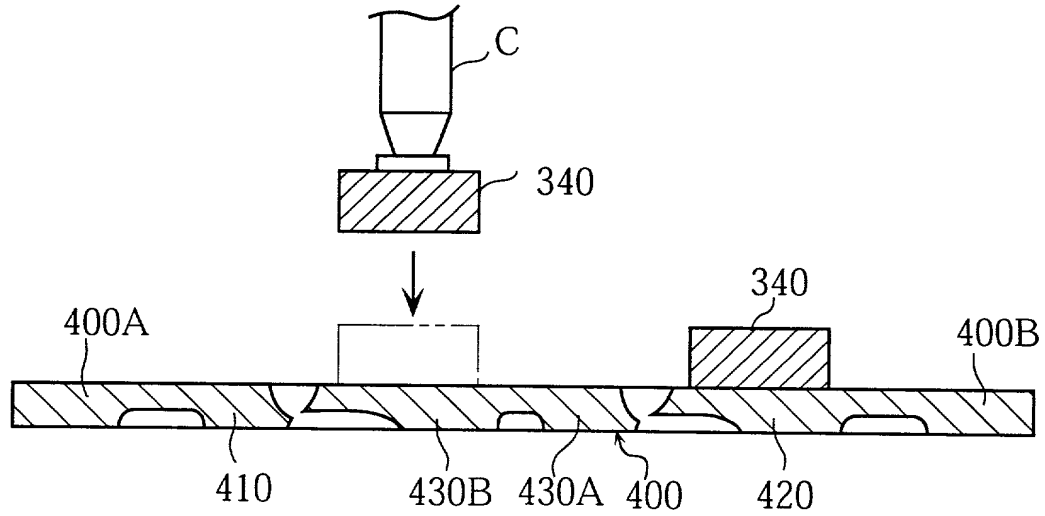


FIG. 17

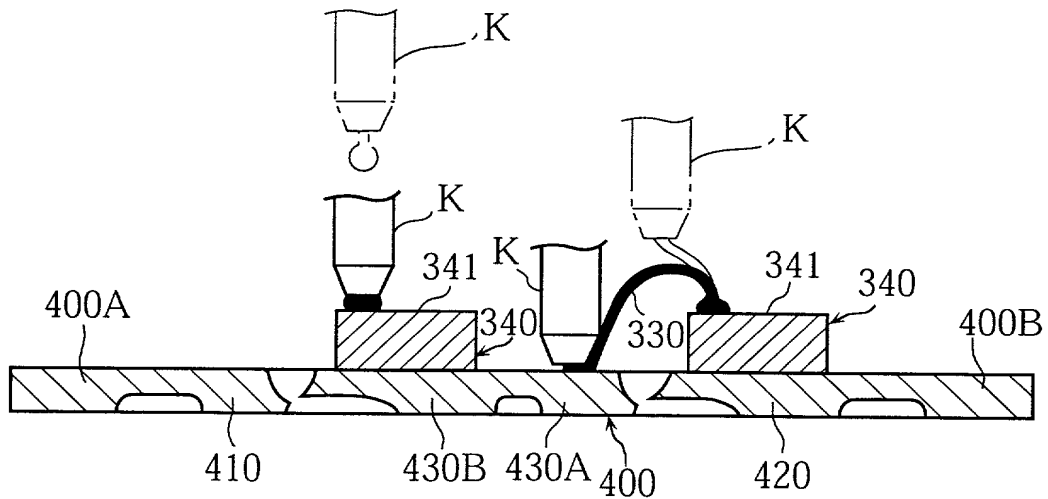


FIG. 18

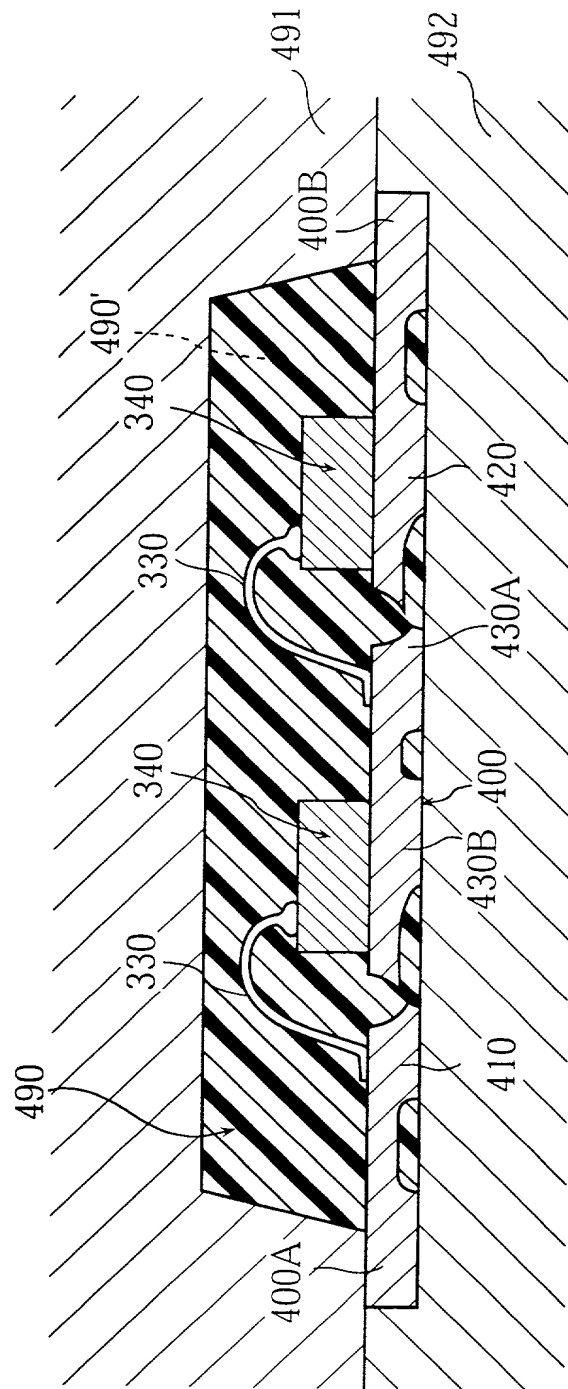


FIG. 19

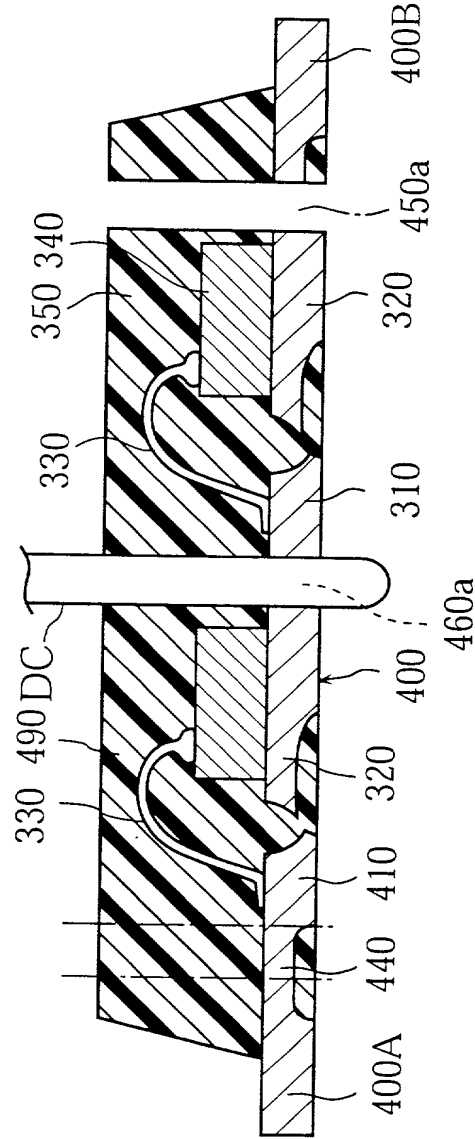


FIG. 24

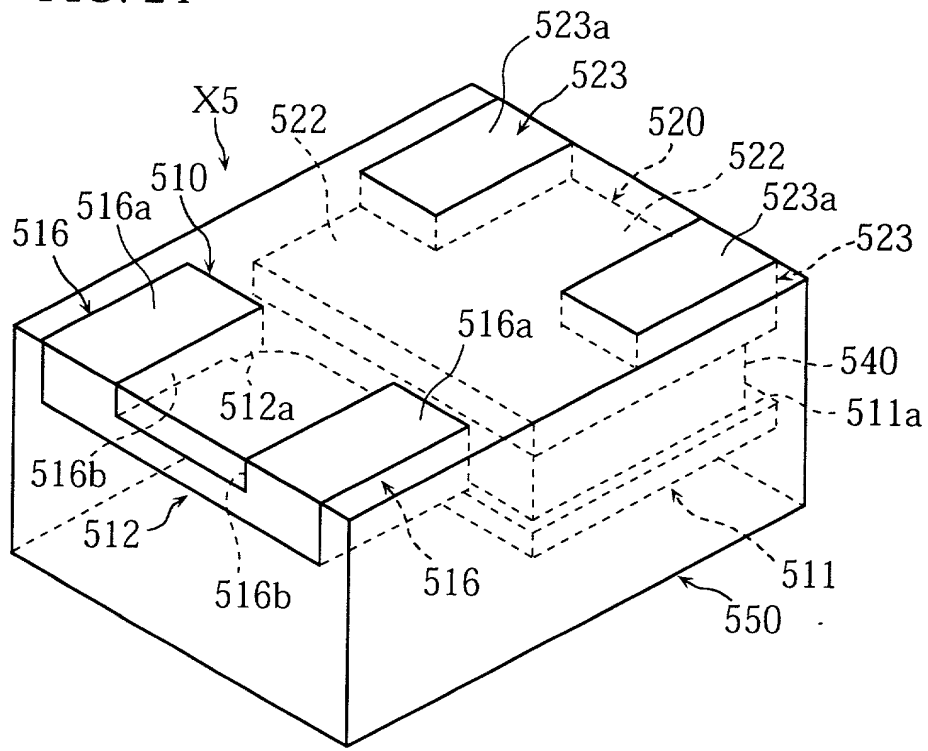


FIG. 25

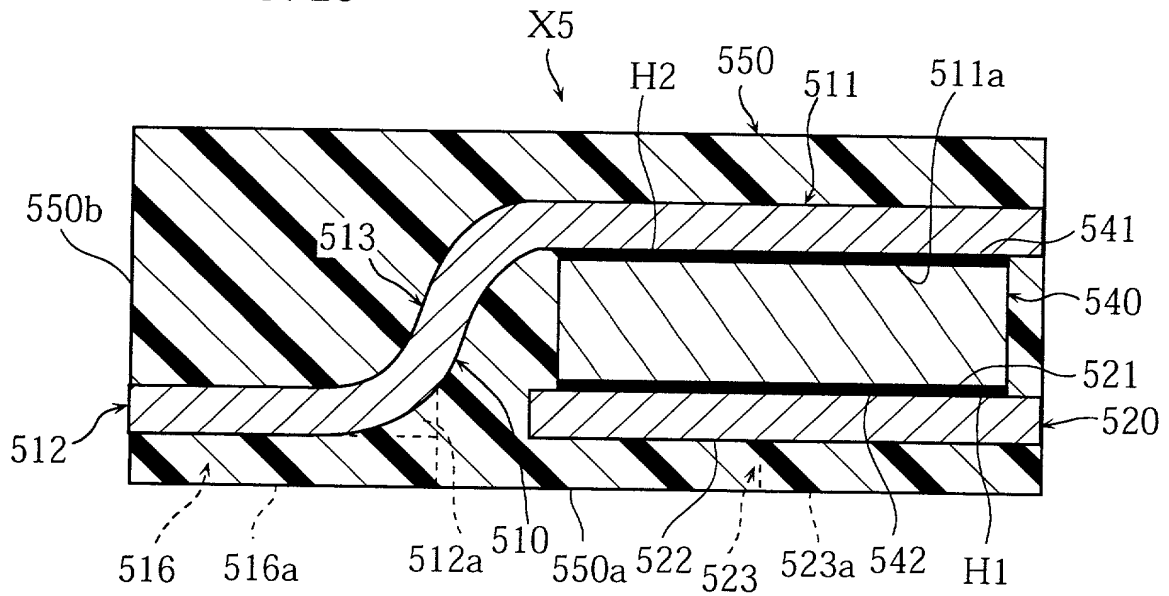


FIG. 26

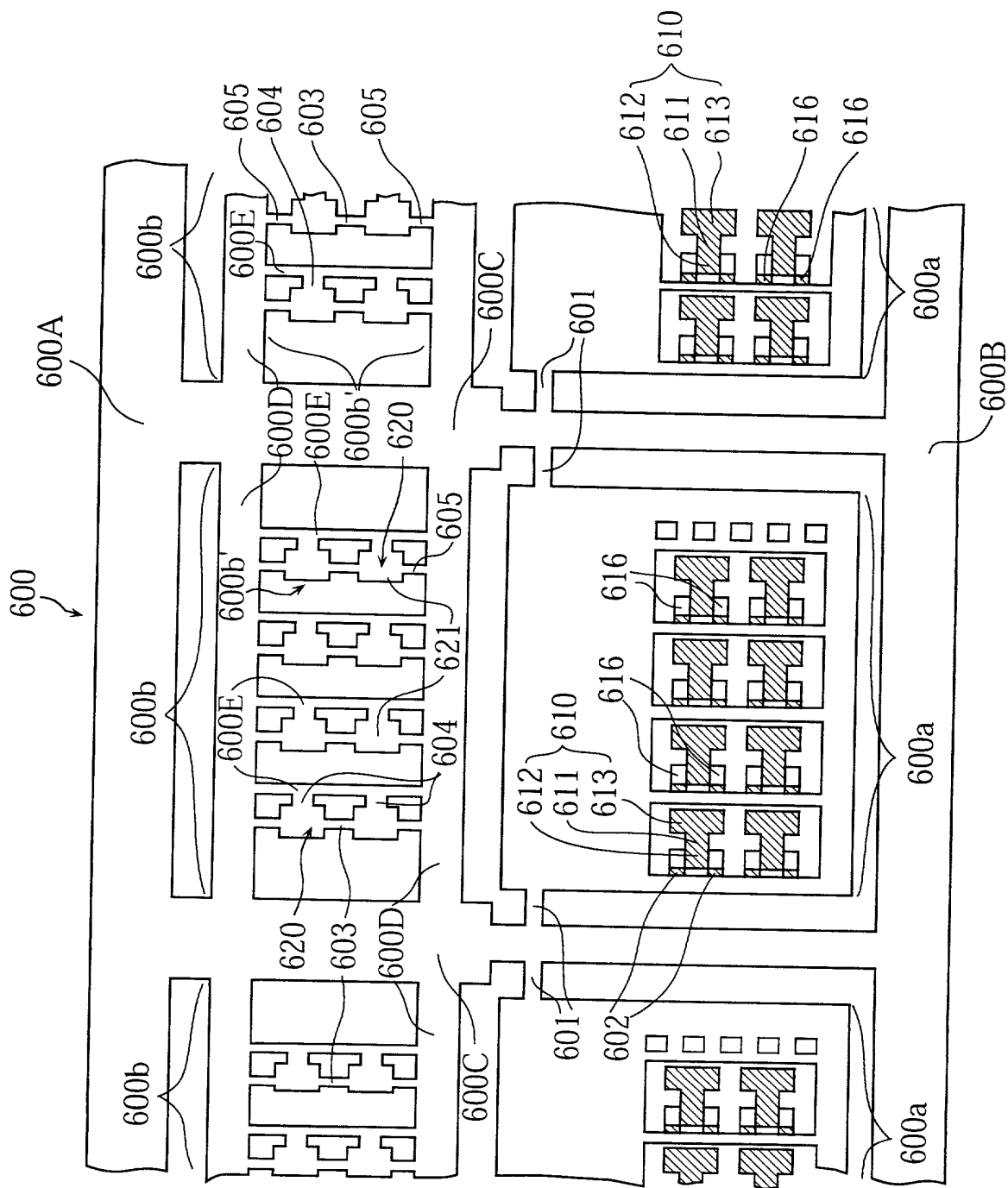


Figure 6 illustrates a semiconductor device in plan and cross-sectional views. The plan view (top) shows a central region 600 with a grid of openings 610, surrounded by regions 600A, 600B, and 600C. The cross-sectional view (bottom) shows the device structure with layers 600A, 600b, and 600D, and various openings and features labeled 601, 602, 603, 604, 605, 611, 612, 613, 621, 622, 623, and 624.

FIG. 28

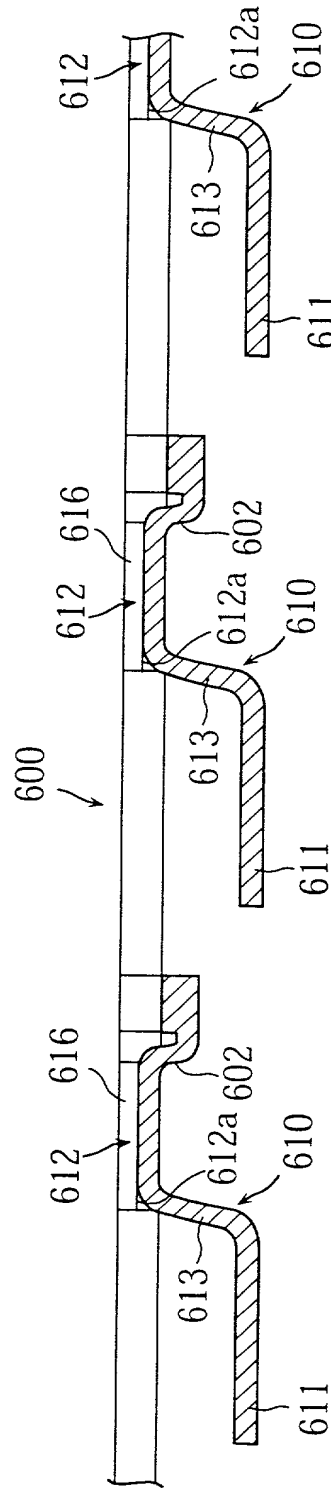
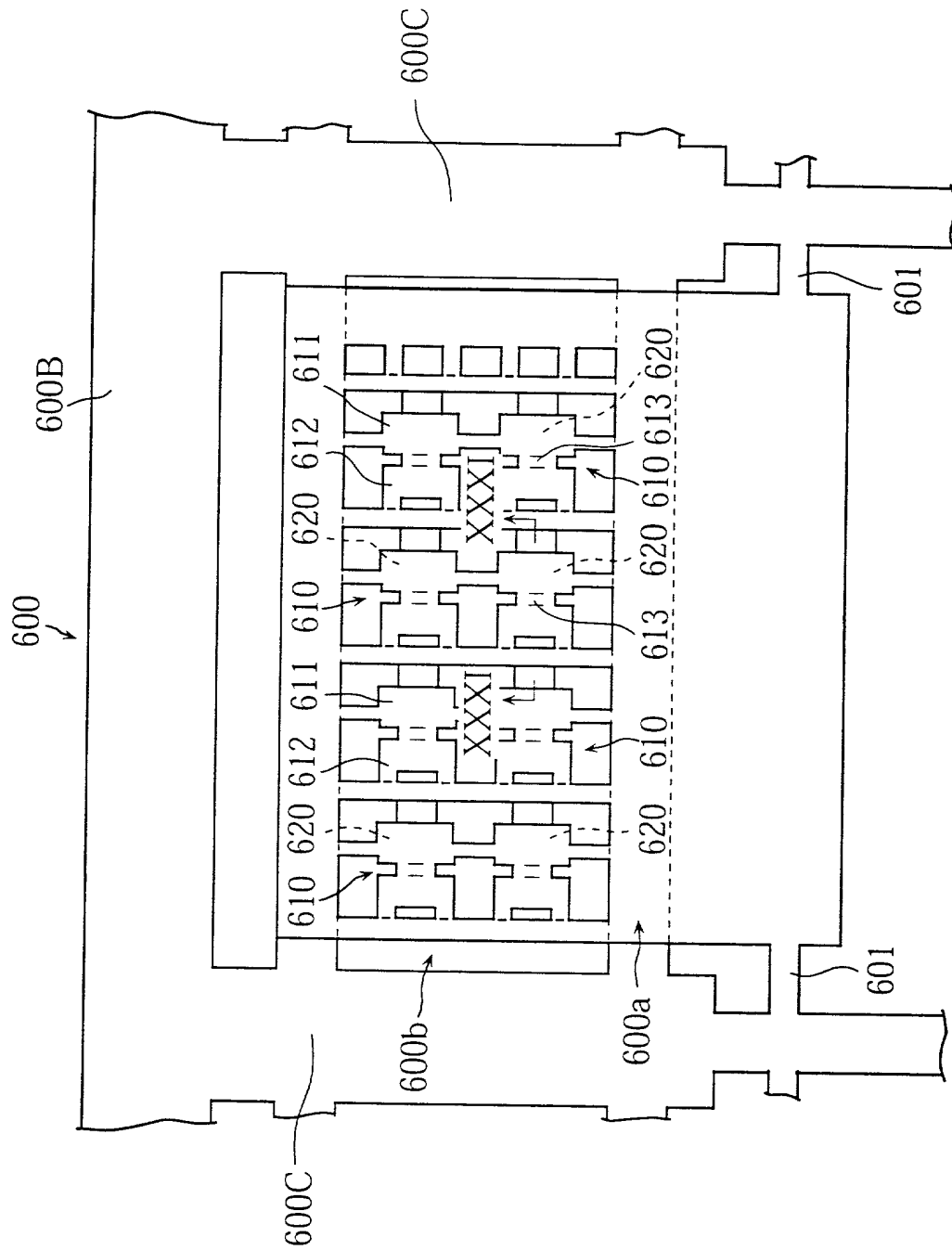




FIG. 30



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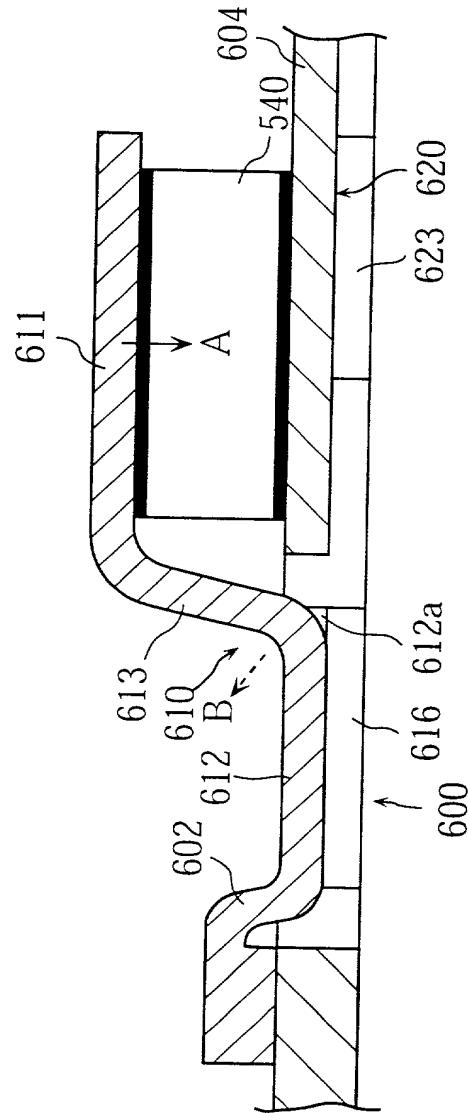


FIG. 34

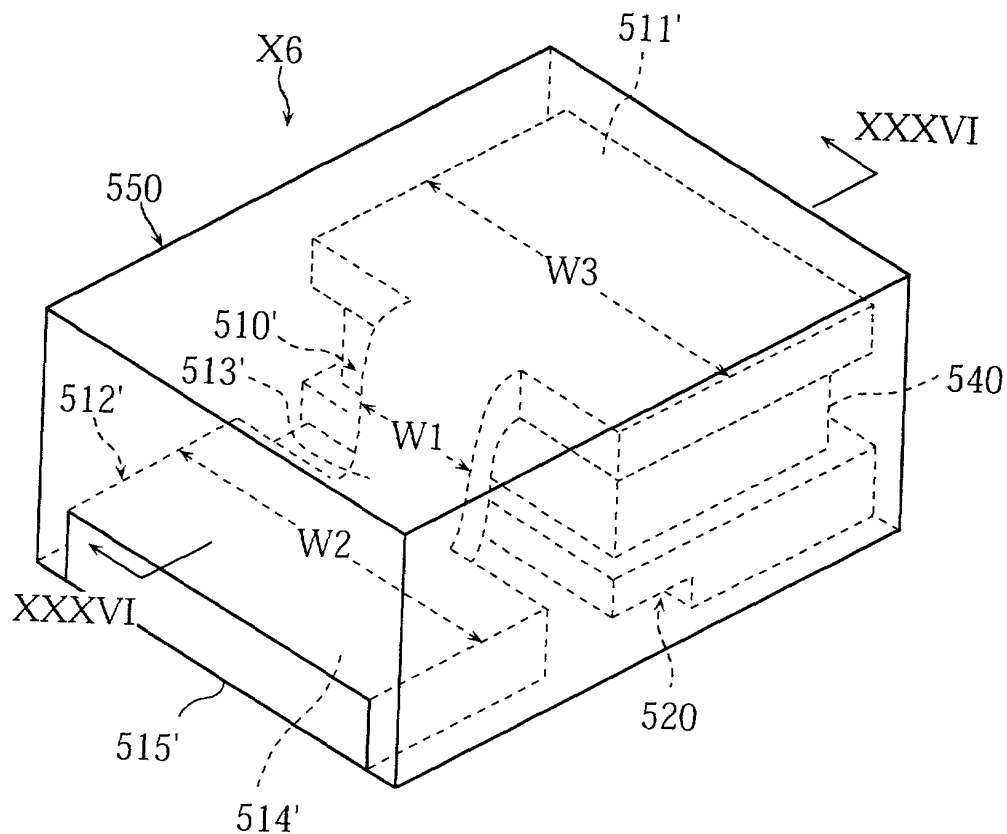


FIG. 35

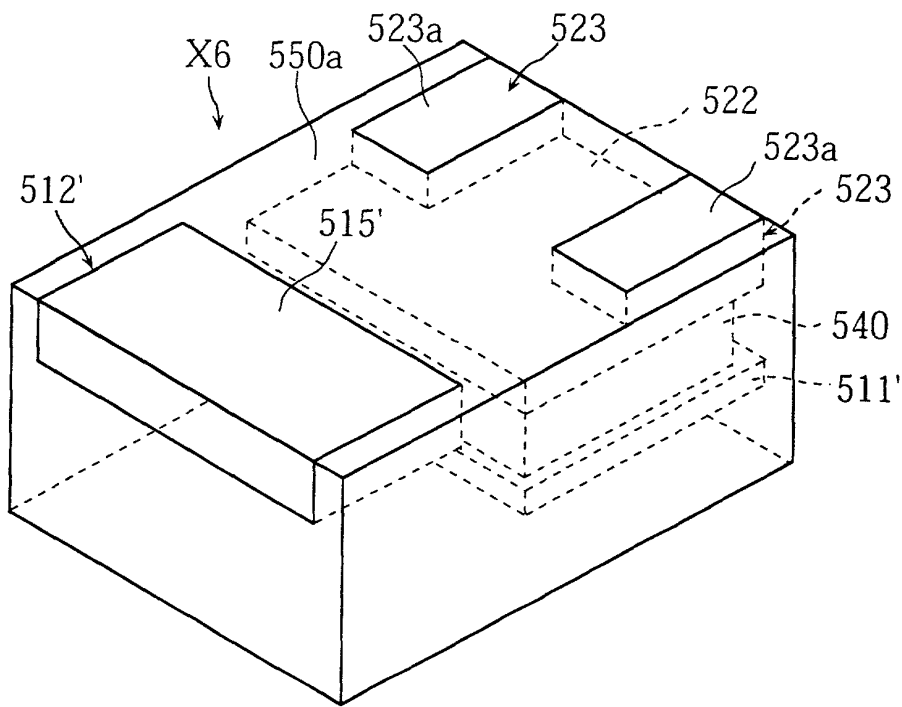
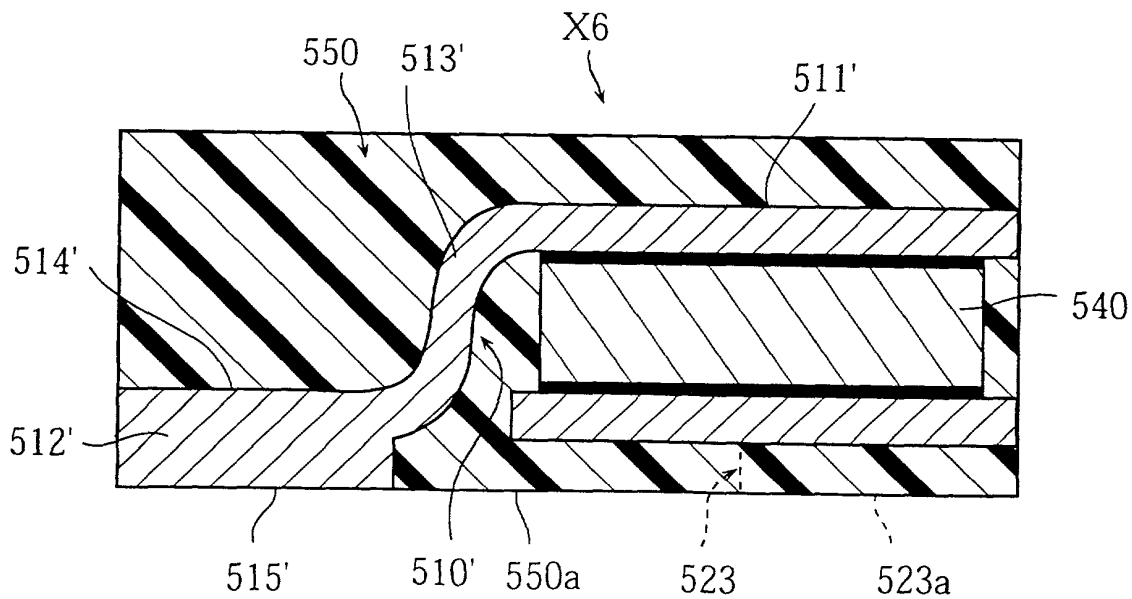


FIG. 36



[illegible]

FIG. 39

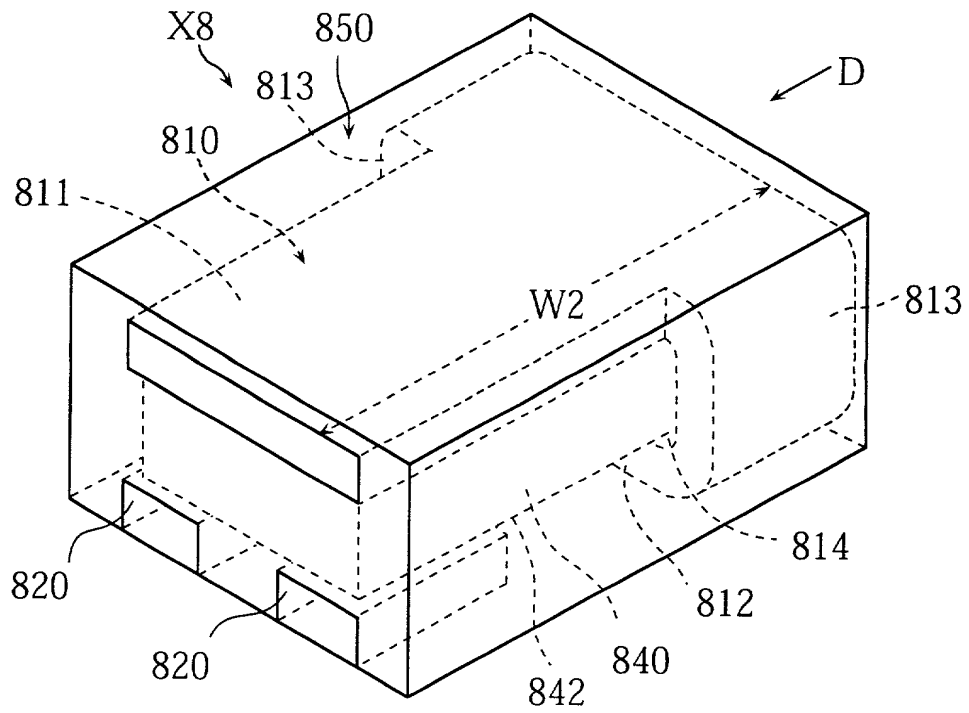


FIG. 40

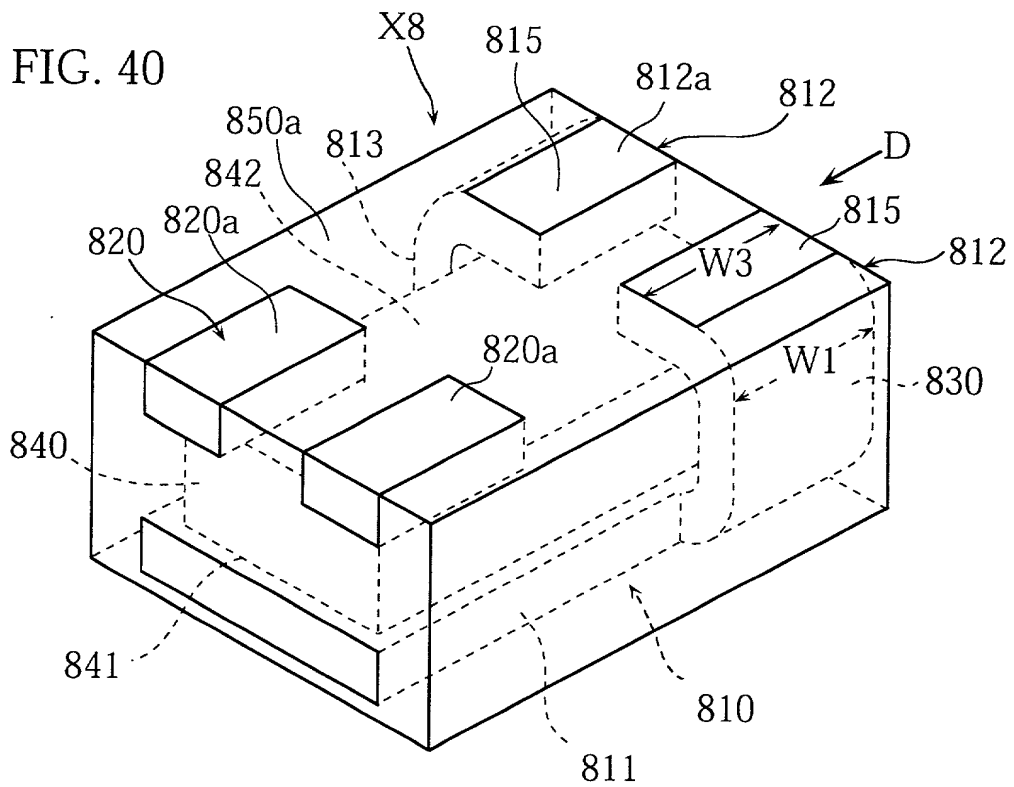


FIG. 42

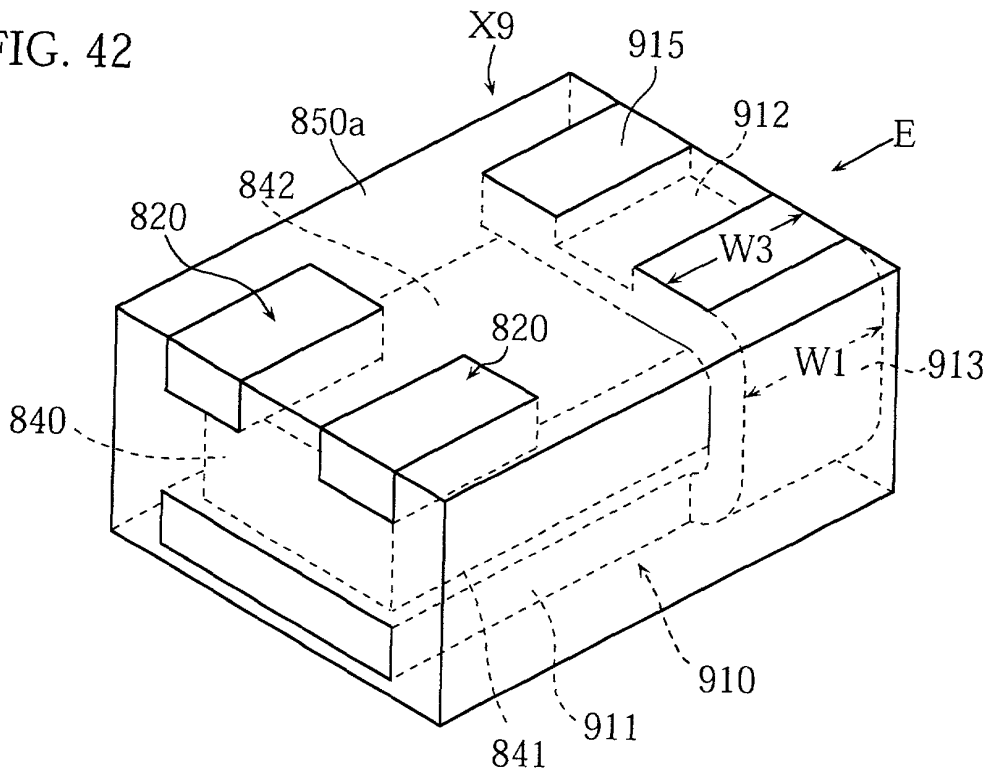


FIG. 43
PRIOR ART

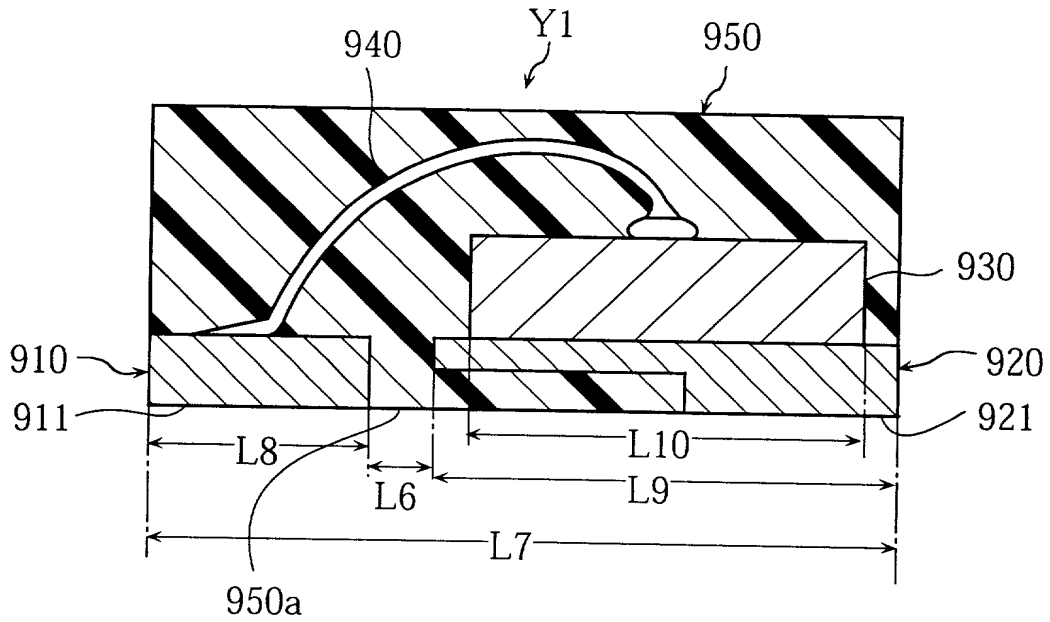


FIG. 44
PRIOR ART

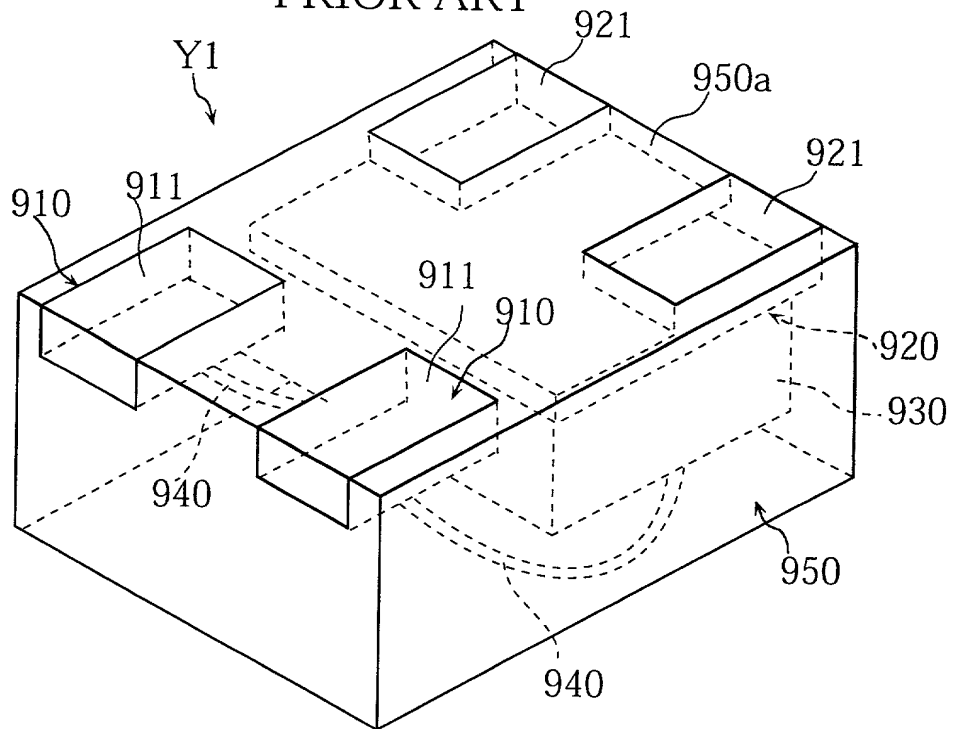


FIG. 45
PRIOR ART

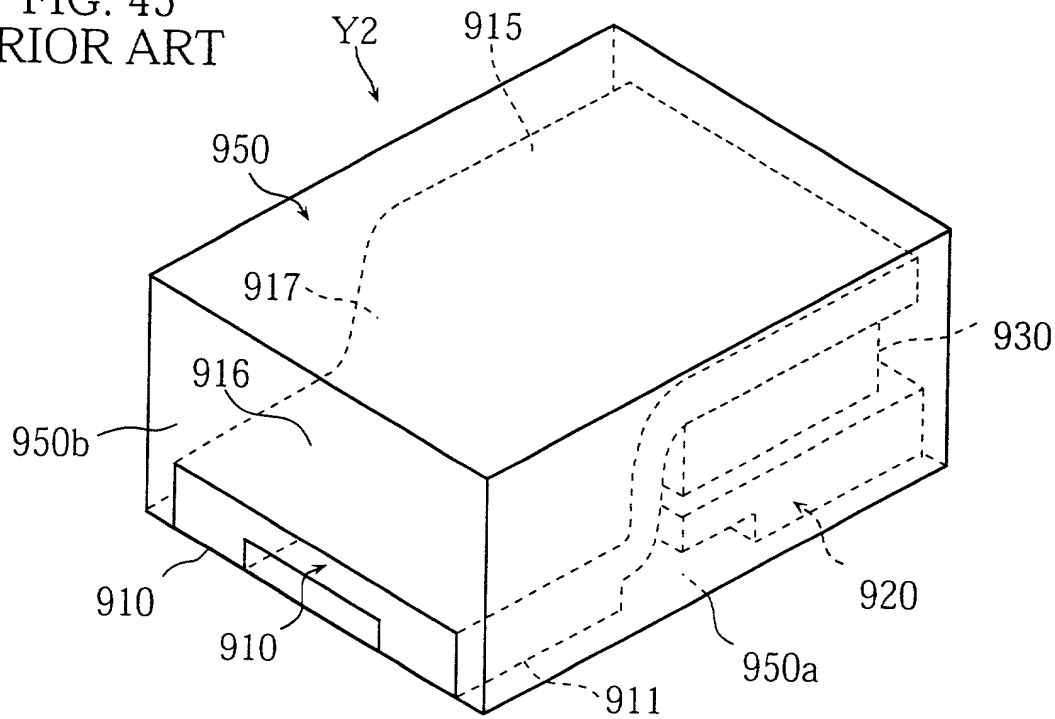


FIG. 46
PRIOR ART

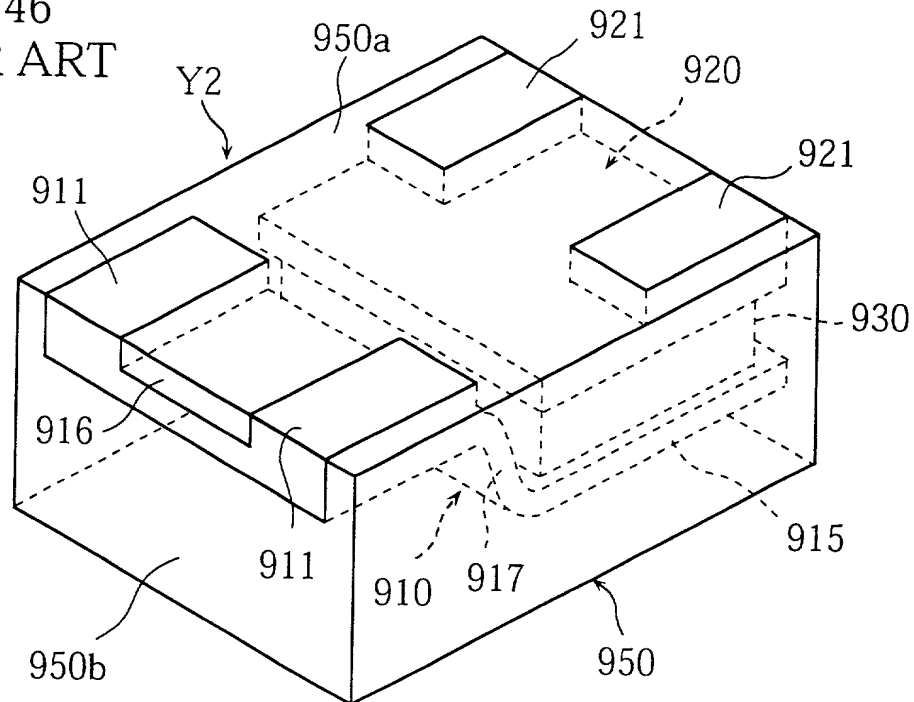
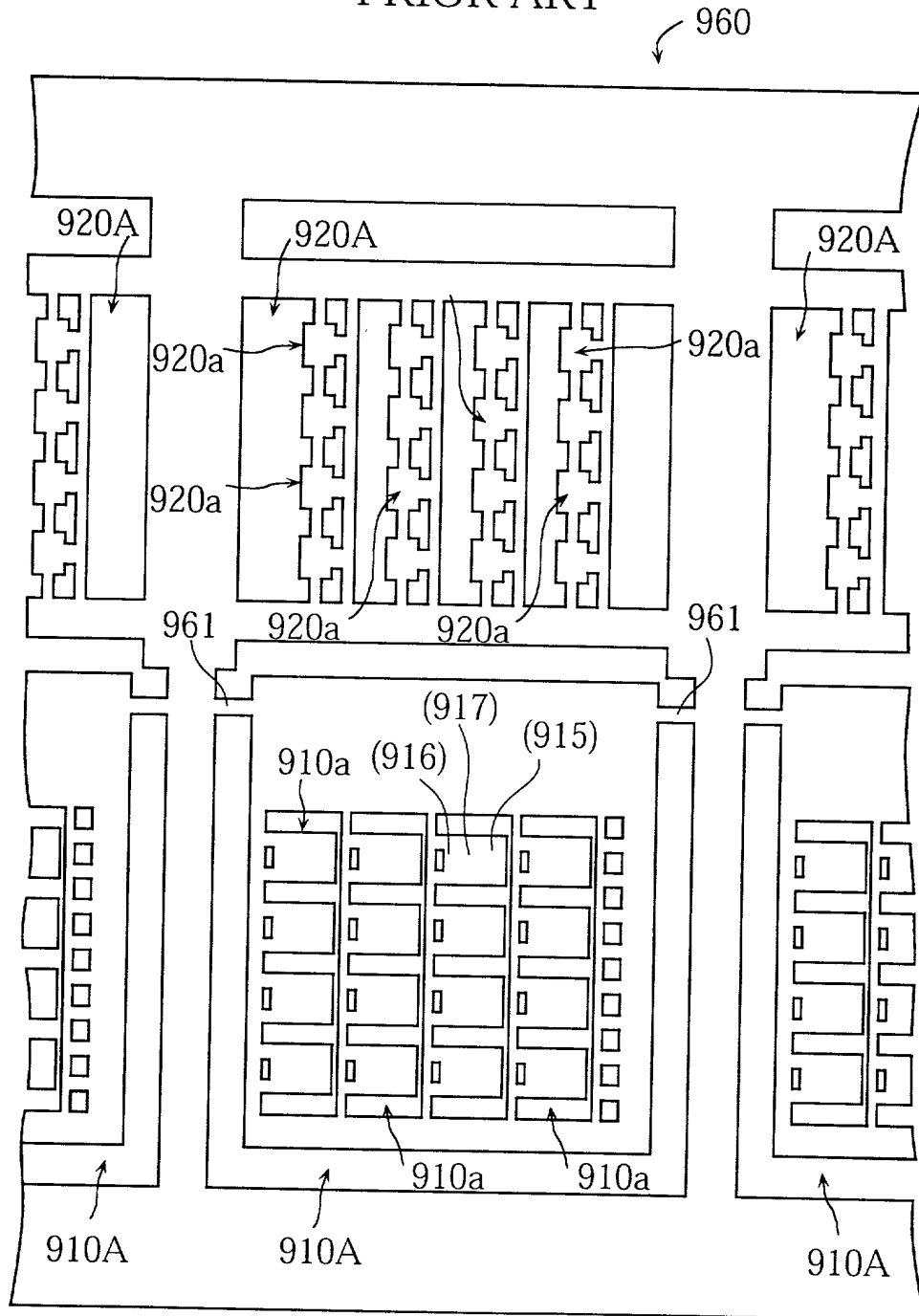


FIG. 47
PRIOR ART



[illegible]